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Applicant: Christoph Wasshuber, et al.

Docket No: TI-31016

Serial No: 10/020,111

Conf. No: 5837

Examiner: Jasmine J. B. Clark

Art Unit: 2815

Filed: 12/14/2001

For: METHODS AND APPARATUS FOR INDUCING STRESS IN A SEMICONDUCTOR  
DEVICE

2815  
#4/Election  
Attord  
8/29/02

ELECTION

Assistant Commissioner for Patents  
Washington, DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)  
I hereby certify that the above correspondence is being  
deposited with the U.S. Postal Service with sufficient  
postage as First Class Mail in an envelope addressed to:  
Assistant Commissioner for Patents, Washington, DC  
20231 on 8-15-02.

Ann Trent  
Ann Trent

Dear Sir:

This election is offered in response to the Examiner's restriction requirement  
mailed July 22, 2002.

Applicants hereby elect to pursue Group I of Claims 1-14, and 23-28, drawn to  
method of fabricating a semiconductor device, without traversing the Examiner's  
restriction requirement.

Respectfully submitted,

Peter K. McLarty  
Peter K. McLarty  
Agent for Applicants  
Reg. No. 44,923

Texas Instruments Incorporated  
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